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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,699	12/01/2003	Francois X. Prinz	24317/82501	2551

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SIDLEY AUSTIN BROWN & WOOD LLP
555 CALIFORNIA STREET
SUITE 2000
SAN FRANCISCO, CA 94104-1715

EXAMINER

BEHM, HARRY RAYMOND

ART UNIT	PAPER NUMBER
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2838

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/725,699

Applicant(s)

PRINZ ET AL.

Examiner

Harry Behm

Art Unit

2838

— The MAILING DATE of this communication appears on the cover sheet with the correspondence address —

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 March 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 2,3,7,15 and 17-21 is/are pending in the application.
- 4a) Of the above claim(s) 15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 2,3,7 and 17-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 September 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application
- ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings received on 9/26/06 are accepted.

Response to Arguments

Applicant's arguments with respect to claims 5-6, 8-14 and 16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

Claim 2 is objected to because of the following informalities: it is unclear whether "a plurality of entries" refers to multiple words in the counter or refers to multiple bits in the counter. For the purpose of examination, the claim language shall be interpreted as meaning multiple bits. Also with respect to claim 2, it is unclear whether "affecting the input of entries" indicates more limitations than altering the counter value. Appropriate clarification is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Corsi (US 5,912,551).

A digital control system for controlling a switch (Fig. 1 10) of a voltage converter, comprising:

a duty cycle generator (Fig. 1 22 and Fig. 2 46,44) that provides a duty cycle [on/off time to gate of power switch] for the switch (Fig. 1 10);

a digital counter [Fig. 1 20 is depicted as a counter, but only flip flops 40 and 42 in Fig. 2 create the counter] that stores a plurality of entries [two bit counter shown], wherein each entry (Fig. 2 Q1z,Q2) can be input [input to 46] to the duty cycle generator (Fig. 1-2 46,44,22) for modifying the duty cycle [gate signal on/off time] in response to a varying load [change in load causes V_{out} to deviate from V_{ref} , which changes the count];

a first comparator (Fig. 1 28) that compares an output voltage (Fig. 1 V_{out}) to a reference voltage (Fig. 1 V_{ref}); and

an algorithm generator (Fig. 1) producing an algorithm that determines the rate of change [duty cycle changed at rate in response to load] of for modifying the duty cycle;

wherein if the first comparator (Fig. 1 28) detects that the output voltage is higher than the reference voltage, the algorithm generator [signal V_{com}] affecting the input of entries from the digital counter [counter reset] into the duty cycle generator, thereby adjusting the rate of change for modifying the duty cycle of the switch [switching prevented].

Claims 2-3, 7 and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Sellers (US 5,189,601).

A digital control system for controlling a switch (Fig. 1 S2) of a voltage converter, comprising:

a duty cycle generator (Fig. 1 22 and Fig. 2 46,44) that provides a duty cycle [on/off time to gate of power switch] for the switch (Fig. 1 S2);

a digital counter (Fig. 4 51) that stores a plurality of entries [8 bit counter shown], wherein each entry (bit) can be input [input to 46] to the duty cycle generator (Fig. 4 5252-57) for modifying the duty cycle [gate signal on/off time] in response to a varying load [change in load causes current to change, which changes the count];

a first comparator (Fig. 4 33') that compares an output voltage (Fig. 4 V_s is output voltage from rectifier 25' and senses current I_s) to a reference voltage (Fig. 4 $+V$ voltage divided); and

an algorithm generator (Fig. 1 21) producing an algorithm that determines the rate of change [duty cycle changed at rate in response to load] of for modifying the duty cycle;

wherein if the first comparator (Fig. 4 33') detects that the output voltage (Fig. 4 V_s) is higher than the reference voltage (Fig. 4 voltage divided $+V$), the algorithm generator (Fig. 4 reset input to 51) affecting the input of entries from the digital counter (Fig. 4 51) into the duty cycle generator, thereby adjusting the rate of change for modifying the duty cycle of the switch [counts].

With respect to Claim 3, Sellers discloses the system of claim 2 further comprising a second comparator (Fig. 4 27').

With respect to Claim 7, Sellers discloses method for producing a desired output voltage (Fig. 4 V_s) comprising:

storing in memory (Fig. 4 51), an indication of a duty cycle [on/off time of power switch] needed for a varying load (Fig. 1 Rld); monitoring the load (Fig. 1 Is charging current);

altering the duty cycle (Fig. 1 23)) at a first frequency (Fig. 1 S1 inactive when $V_s > \text{ref}$) to produce the desired output voltage [V_s tracks ref] based upon the indication; and

if a change in the load is detected (Fig. 4 27'), changing the frequency (Fig. initiate switching) of alteration of the duty cycle;

wherein if the load increases [requires additional charging current], the frequency of alteration is increased [begin switching], thereby minimizing a dip in the output voltage [increase charging current to increase output voltage to load].

With respect to Claim 17, Duffy discloses the method of claim 7 wherein monitoring the load (Fig. 1 Is) comprises usage of two (Fig. 4 27'33') or more comparators.

With respect to Claim 18, Duffy discloses the method of claim 17 wherein the two (Fig. 4 27',33') or more comparators each have a different reference (Fig. 4 Vref and second reference voltage divided +V).

With respect to Claims 19-21, Duffy discloses a voltage converter. See claims 7 and 17-18 for item matching.

Claims 7 and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Brooks (US 6,356,063).

With respect to Claim 7, Brooks discloses method for producing a desired output voltage (Fig. 3 Vref) comprising:

storing in memory (Fig. 8 D1-Dn), an indication [command indicates duty cycle since the duty cycle must approach the command in steady state] of a duty cycle [on/off time of power switch] needed for a varying load; monitoring the load (Fig. 3 V-out feedback);

altering the duty cycle (Fig. 3 VPH) at a first frequency (Fig. 3 PWM alters duty cycle at first frequency in response to error signal Vc) to produce the desired output voltage [output voltage tracks command] based upon the indication; and

if a change in the load is detected (Fig. 3 300 detects output voltage exceeds window), changing the frequency (Fig. 3 INJ modifies Vc changing the frequency) of alteration of the duty cycle;

wherein if the load increases [increasing load causes decreasing output voltage], the frequency of alteration is increased [increasing load detected at comparator Fig. 6 604], thereby minimizing a dip in the output voltage [comparator 604 forces power switch active, see Fig. 9C].

With respect to Claim 17, Brooks discloses the method of claim 7 wherein monitoring the load (Fig. 6 V-OUT feedback) comprises usage of two (Fig. 6 602,604) or more comparators.

With respect to Claim 18, Brooks discloses the method of claim 17 wherein the two (Fig. 6 602,604) or more comparators each have a different reference (Fig. 6 output

of buffer amplifier 600 and different reference of voltage divided difference between buffer and comparator 604 output).

With respect to Claims 19-21, Brooks discloses a voltage converter. See claims 7 and 17-18 for item matching.

Claims 7 and 17-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Duffy (US 2002/0171985).

With respect to Claim 7, Duffy discloses method for producing a desired output voltage (Fig. 12 V_o) comprising:

storing in memory (Fig. 8 730), an indication [error voltage used to generate duty cycle] of a duty cycle [on/off time of power switch] needed for a varying load (Fig. 6 530); monitoring the load (Fig. 6 $V_{SEN P}$, $V_{SEN N}$, A_{TRHC} , A_{TRLC});

altering the duty cycle (on/off switching of power switches) at a first frequency (Fig. 14 initial frequency in which transient support (Fig. 6 540) is not used) to produce the desired output voltage (Fig. 6 572) based upon the indication; and

if a change in the load is detected (Fig. 9 910 comparator detect outside of window), changing the frequency (Fig. 14 period extended after load changes at 1450) of alteration of the duty cycle;

wherein if the load increases (Fig. 14 1450), the frequency of alteration is increased (Fig. 6 540 quickly activates switches), thereby minimizing a dip in the output voltage [increased output current minimized output voltage drop].

With respect to Claim 17, Duffy discloses the method of claim 7 wherein monitoring the load (Fig. 6 530) comprises usage of two (Fig. 9 910) or more comparators.

With respect to Claim 18, Brooks discloses the method of claim 17 wherein the two (Fig. 6 602,604) or more comparators each have a different reference (Fig. 6 $V_{ref} + \Delta b1, V_{ref} - \Delta b1$).

With respect to Claims 19-21, Duffy discloses a voltage converter. See claims 7 and 17-18 for item matching.

Allowable Subject Matter

The indicated allowability of claim 2 is withdrawn in view of the newly discovered reference(s) to Corsi (US 5,912,551) or Sellers (US 5,189,601). The indicated allowability of claim 7 is withdrawn in view of the Brooks (US 6,356,063) or Duffy (US 2002/0171985).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry Behm whose telephone number is 571-272-8929. The examiner can normally be reached on Business EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Karl Easthom can be reached on 571-272-1989. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.


KARL EASTHOM
SUPERVISORY PATENT EXAMINER